AN231K04-DVLP3 – AnadigmApex Development Board

1.0 Overview

The AnadigmApex development board is an easy-to-use platform designed to help you get started with implementing and testing your analog designs on the AnadigmApex FPAA silicon devices.

While the device on this development platform is an AN231E04 device, you can use this board to implement all of your AN131E04 and AN231E04 designs. The design software - AnadigmDesigner®2 – can use the AN231E04 device on board to emulate the AN131E04 device thus enabling instant prototyping of your design for either device in the AnadigmApex device family.

Note : the physical device on this board is a 7x7mm TQFP, the volume production device is housed in a 7x7mm QFN package.

This manual provides an overview on how to effectively use this board to implement your analog design. But first, here are some salient features of the AnadigmApex development board:

- Small footprint – 4.2 inches square
- Large breadboard area around the AN231E04 device
- Header pins for all the FPAA device analog I/Os
- Ability to separate, electrically and physically, the digital section
- Two circuit footprints for configuration as Rauch filters, single to diff converters, level shifters etc
- Daisy chain capability – that allows multiple boards to be connected to evaluate multi-chip systems
- Standard PC serial interface for downloading AnadigmDesigner®2 circuit files
- On-board 16-MHz oscillator module

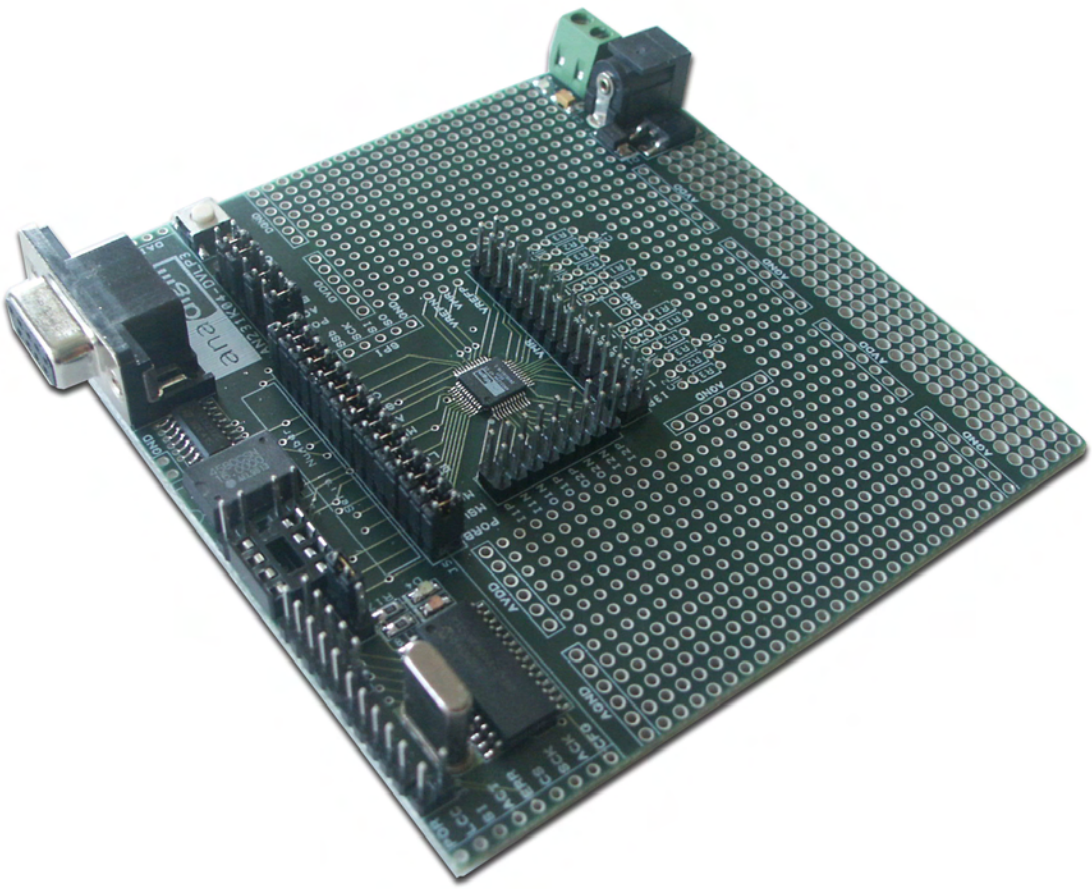

Figure 1: AnadigmApex Development Board

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2.0 Layout

Figures 2 shows the layout of the board allowing easy location of all the components, power connections and jumpers.

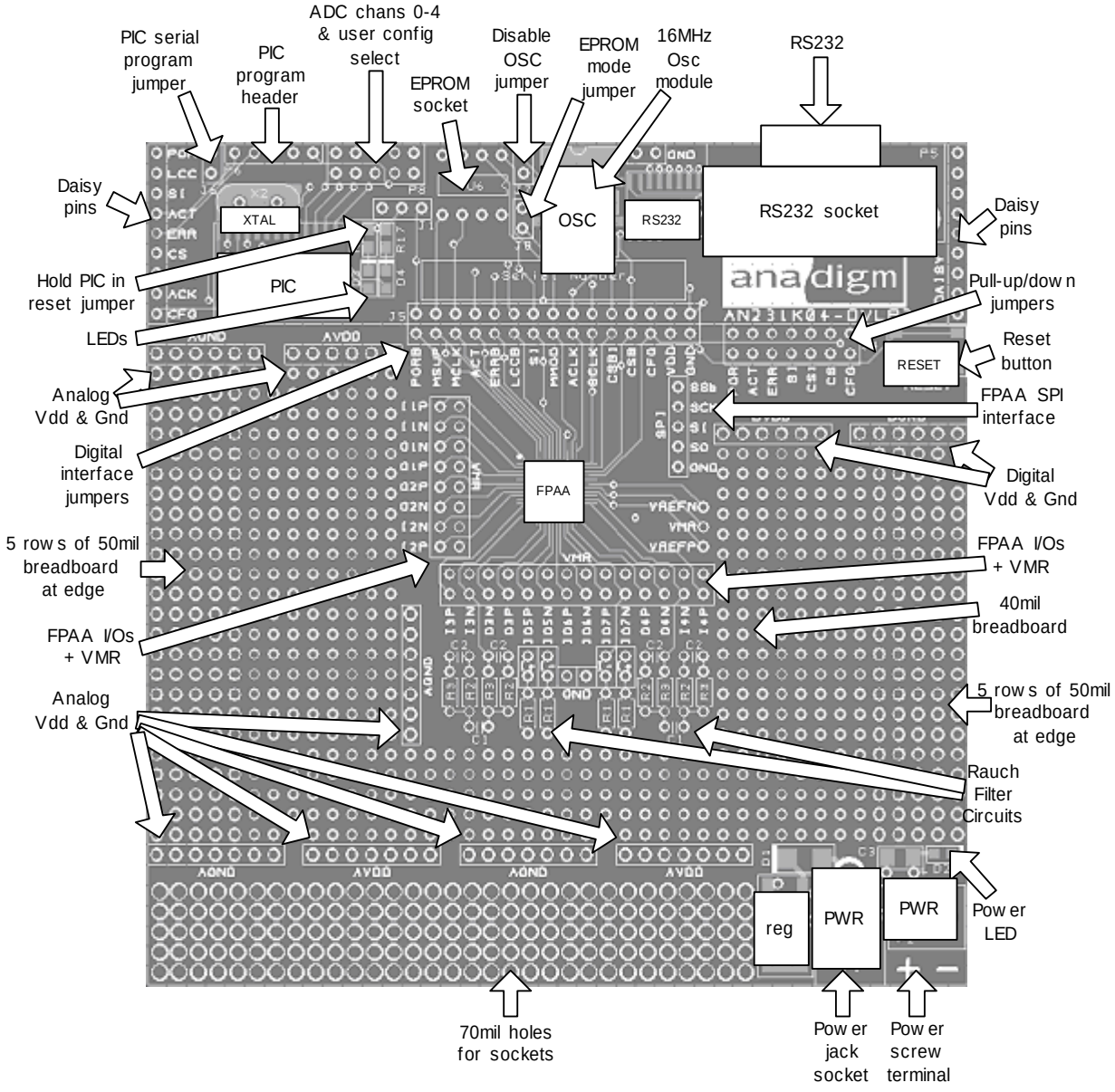


Figure 2: Top-level layout of the AnadigmApex development board

3.0 Powering up the AnadigmApex Development Board

The options for powering up the board are as follows:

- Connect a transformer with centre voltage between +4V and +12V to the jack socket input, OR
- Connect wires from a single precision, regulated supply to the on-board 2-way terminal with the voltage set to between 4V and 12V.
- Anadigm recommends the use of a standard supply regulator or d.c. power supply 6 or 9 volt d.c. regulated output.

NOTE: the board is protected against connection to a supply with the wrong polarity

WARNING: the board should not be powered with more than 12.5V

There is a green LED to indicate that the board is successfully powered up. The board should take approximately 25mA when first powered up and before the FPAA is configured. The current after the FPAA is configured depends very much on the circuit programmed into the FPAA.

4.0 Programming the Board

Once the board has been powered up, simply connect the board to the serial port of a PC using a standard RS232 cable. Open AnadigmDesigner®2 on the PC, create a circuit and click on Configure. If configuration is successful, the green LED next to the PIC in the digital section will light. If the red LED lights then the configuration failed. If this happens then check the supply to the board and check that the pins marked AVDD have +3.3V on them. Also check that the jumpers are in their default state (see figure 3 in section 8). Press the reset button and try again.

If configuration was successful then the circuit created in AnadigmDesigner®2 will be programmed into the FPAA. The analog inputs and outputs can be accessed via the header pins that surround the FPAA. Note that the outer pins are connected to the analog I/Os, the inner pins are all connected to VMR which is at analog signal ground (+1.5V).

5.0 Evaluating Multi-chip Designs – Daisy Chaining

Figure 3 shows an example of how to chain 2 boards together. More boards can be chained using the instructions shown in this figure.

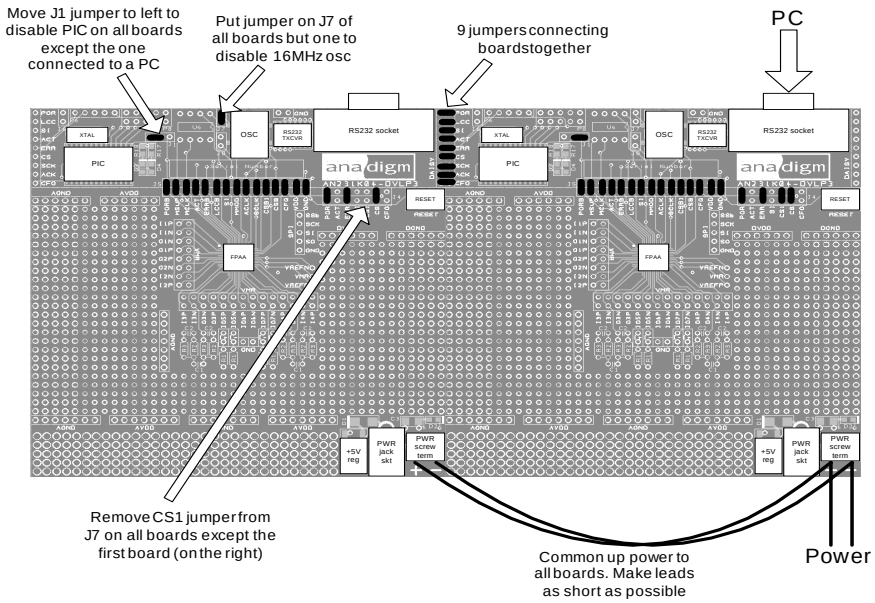


Figure 3: Positions of Jumpers and Default Settings

6.0 Other Features

V_{REF} Pins

The 3 reference pins on the FPAA device – VMR (+1.5V), VREFP (+2.5V) and VREFN (+0.5V) – have been connected via the p.c.b. tracks to the 3 holes to the right of the FPAA. In addition, VMR is available on 2 rows of pins that are adjacent to the analog I/Os. These reference voltages are not designed to provide current.

Header Pins

All of the analog I/Os of the FPAA are brought out to header pins for easy connection. Next to these header pins is a second row of header pins connected to VMR (+1.5V). This allows the user to connect any FPAA analog I/O to VMR using shorting jumpers, resistor jumpers or capacitor jumpers.

EPROM

There is an SPI EEPROM socket in the digital section of the board. To put the board into EPROM mode:

1. Put a jumper onto J8 which sits right next to the EPROM socket, and
2. Put a jumper on J4 in the position marked SI so that this pin is connected to a pull-down.
3. Make sure that there are jumpers on J5 in the positions marked GND, VDD, CFG, ACLK, SI, MCLK and MSUP (it is OK to put jumpers in all positions of J5).

Press the “reset” button to download the circuit from the EPROM into the FPAA.

Reset Button

There is a reset button near the upper right corner of the board. This resets both the FPAA and the PIC (unless the PORB jumper is removed from J5 or the J1 jumper is in the left position).
In EPROM mode, press the reset button to load the circuit from the EPROM into the FPAA.

SPI Port

There is an SPI port for direct control of the FPAA by an external SPI controller. Note that all the jumpers should be removed from J5 when the SPI port is used. (see the AN231E04 FPAA specification and use guide for details of this SPI connection)

Digital Section

The digital section of the evaluation board is provided only so that there is a convenient (serial) interface from the board to a PC to enable direct configuration (instant prototyping) of the FPAA from AnadigmDesigner®2 software, normal use of the FPAA does not require this digital interface, the FPAA can be programmed directly from an SPI interface. It is convenient when first developing an analog circuit within the FPAA to have the direct interface to AnadigmDesigner®2, when the circuit(s) are implemented into a final design either a host uP (or DSP) or an EEPROM is normally used to store and configure the FPAA.

The digital section of the board includes an RS-232 transceiver and a PIC microcontroller (to perform serial ASCII to bit conversion). It also includes a green LED (to indicate successful configuration), and a red LED (to indicate failed configuration

The digital section sits along the top side of the board and is connected to the rest of the board by a set of jumpers J5. It is possible to cut away the digital section to leave a purely analog board with header pins on the edge to provide an external digital interface.

If the digital section of the development board is removed or ignored (by pulling jumpers J5), the FPAA can be configured directly using any processor with an SPI interface (or port configured with appropriate signals) by connecting signals directly to the FPAA side of J5 or by connecting to the set of pins marked “SPI”. Full dynamic control of the FPAA’s analog circuitry can be realised under software control via this connection.

Note

Anadigm® does not recommend any specific processor/controllers – our products work with most processors.

Anadigm® recommends that our customers use their own processor development boards and connect via jumper J5 to Anadigm’s FPAA for fully dynamic control of the FPAA, in preference to re-engineering the digital section of this development board.

7.0 Jumpers

Table 1 shows a complete list of the jumpers on the board and figure 4 shows their positions.

Jumper	Function	Default State	Default Condition
J1	This jumper allows the MCLRb pin of the PIC to either be connected to the PORb pin of the FPAA or to be grounded. Grounding the MCLRb pin tristates all of the PIC I/Os and thus allows connection of another controller to the digital pins of the FPAA. Useful for daisy chaining boards where one PIC controls 2 or more FPAAs.	Jumper to right	MCLRb pin of PIC is connected to PORb pin of FPAA
J4	Connects pull-ups and downs to some of the FPAA digital pins, or ties CS_B1 low. A jumper in place connects the pull-up/down in the following way: POR – 10k pull-up on PORb ACT – 10k pull-up on ACTIVATE ERR – 10k pull-up on ERRb SI – 10k pull-down on SI CS1 – ties CS_B1 low CS – 10k pull-down on CS_B CFG – 10k pull-up on CFGFLG	Jumpers on POR, ERR, CS1 and CS	PORb is pulled high, ERRb is pulled high, CS_B1 is tied low and CS_B is pulled low.
J5	Connects the digital section to the analog section	All 15 jumpers should be on.	Fully connects power, ground and all FPAA digital signals to the digital section.
J6	Allows serial download of software to PIC via the RS232 port. Press reset after placing a jumper on J6 and then use Tera Term Pro to download the new software.	Jumper off	Not in software download mode
J7	A jumper on J7 will disable the 16MHz oscillator module and tristate its output. This means that the ACLK pin of the FPAA will not be clocked. Useful in daisy chaining boards where the ACLK pin of 2 or more FPAAs should be driven by one source.	Jumper off	16MHz oscillator enabled
J8	A jumper on J8 enables EPROM mode.	Jumper off	Board in micro mode.

Table 1: Summary of Development Board Jumpers

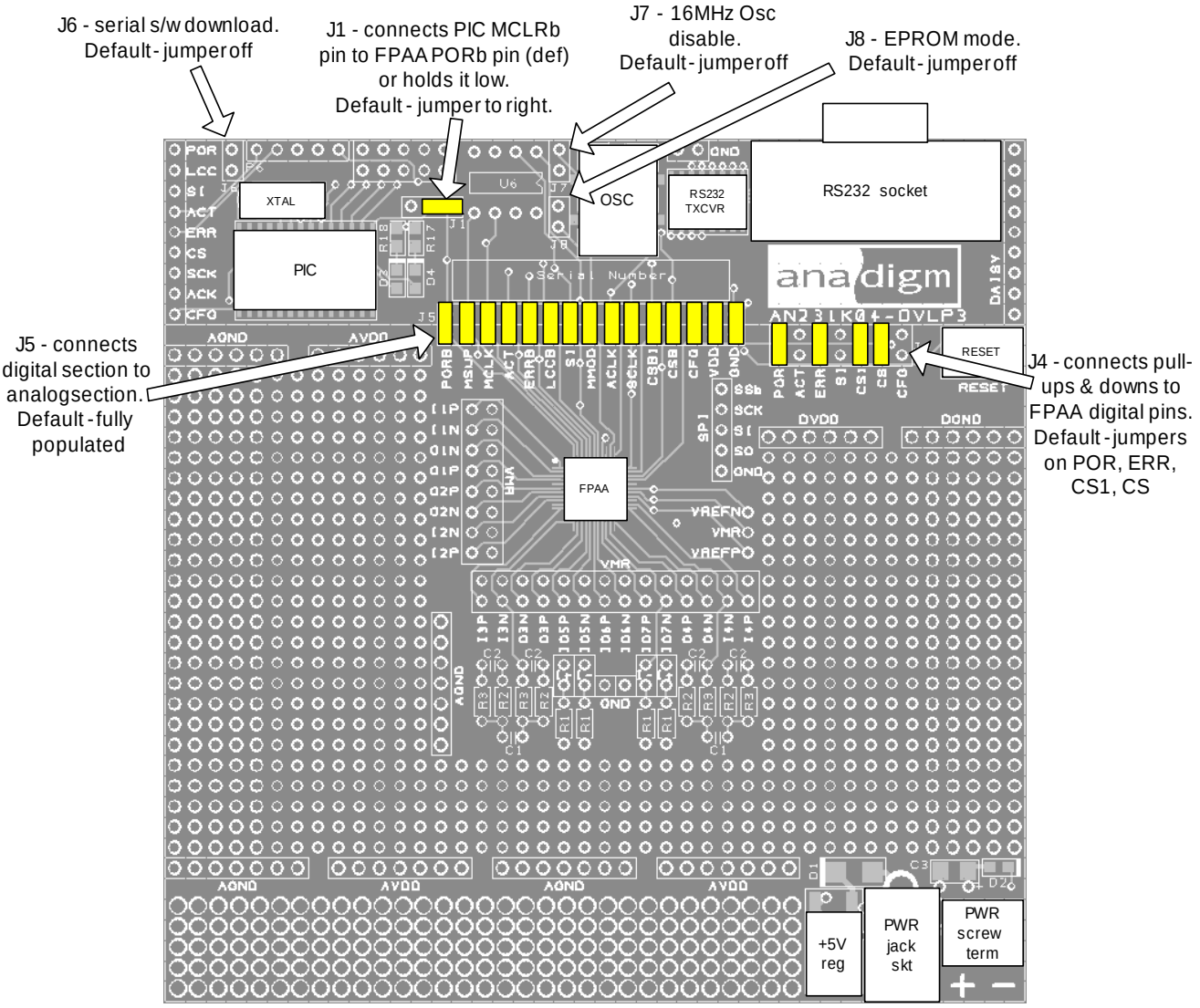
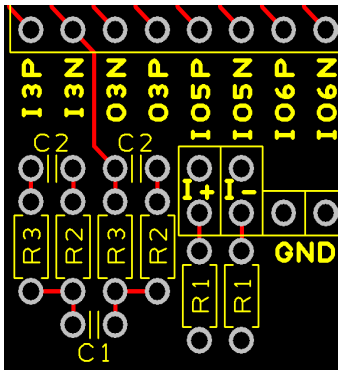


Figure 4: Positions of Jumpers and Default Settings

8.0 Rauch Filters

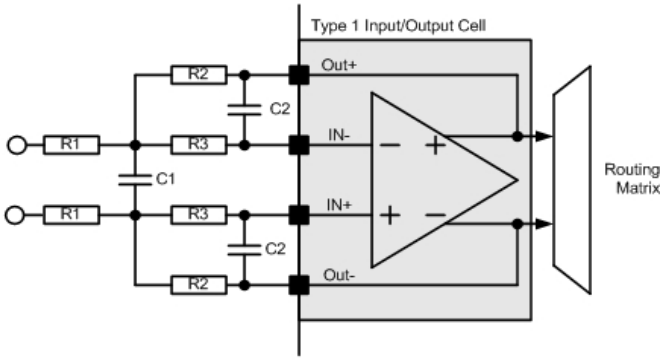
The AN231K04 printed circuit board has an available option for you to use to add Rauch filters, at either the analog input signal path, output signal path or neither. Figure 5, details two suggested Rauch filter circuits.



These can be used easily implemented by adding appropriate components to the p.c.b. this picture of the p.c.b show's an example of one of two p.c.b. layouts, for resistor and capacitor placement.

The default signal connection is directly to the header pin connected to the AN231E04 FPAA. To use these filters add the correct components and connect the signal input or output appropriately.

The math associated with a typical low pass input filter is also provided here.



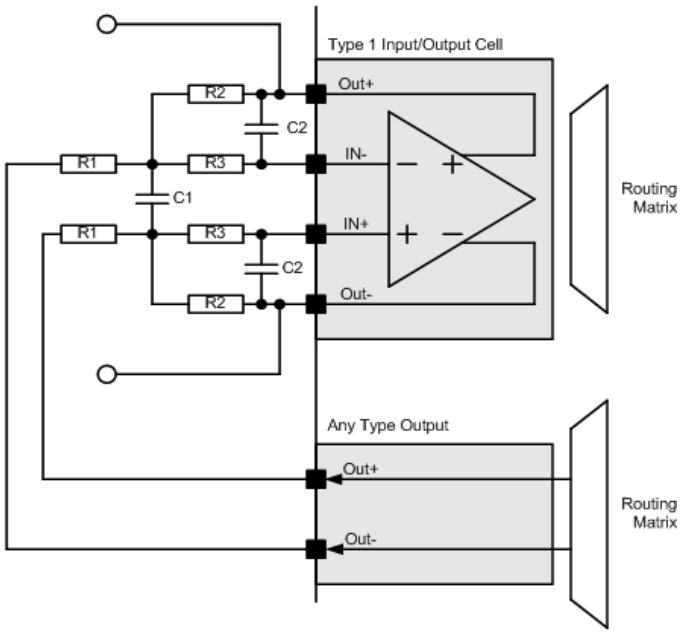
Type 1 I/O Configured as an Input with Anti-aliasing Filter

For low pass response:

H(s) = 1/((R1/R2)+ (sC2(R1+R3+(R1*R3/R2)))+ (s^2R1R3C1C2))

R1 = R2 = 2R3 = 2R
And
C1 = 4C2 = 4C

Fp = 1/(4pie RC(SQRT 2))



Type 1 I/O Configured as a Smoothing Filter for an Output Cell

Re-arranging these equations for low pass filter

R1 = Rin;

R2 = G*Rin;

R3 = G*Rin;

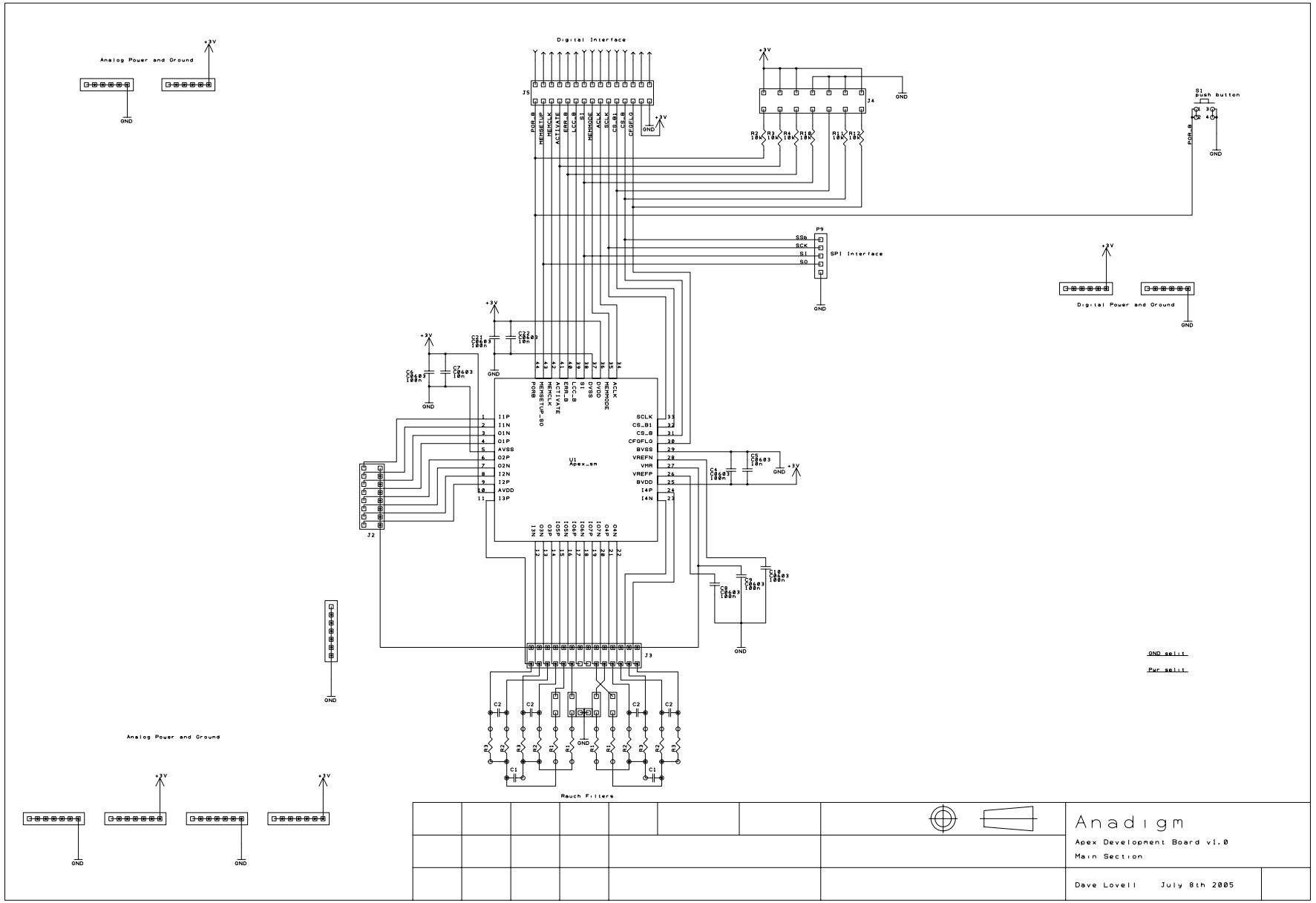
C1 = [Q*(G-2)]/(4*pi *Fo*Rin);

C2 = (2*C1)/[Q*(G-2)]^2

Figure 5: Suggested Rauch filter circuits

9.0 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC Power Supply 3.5mm jack socket	V_{jack}	4		12.5	V	DC voltage only Centre pole is positive, outer sleeve is ground
DC Power Supply Screw terminal "+" post	V+	4		12.5	V	DC voltage only Voltage is relative to "Gnd" post
FPAA Input Voltage	F_{in}	-0.5	+3.6		V	Direct input to FPAA on analog IO header pins or digital pins (J5)
FPAA Output Voltage	F_{out}	-0.5	+3.6		V	Direct output from FPAA on analog IO header pins or digital pins (J5)
RS-232 Input Voltage	R_{in}	-30	+/-10	+30	V	Standard RS-232 signal levels
RS-232 Output Voltage	T_{out}	-15	+/-10	+15	V	Standard RS-232 signal levels
Operating Temperature	T_{op}	10		50	^{o}C	Ambient Operating Temperature
Storage Temperature	T_{stg}	-20		70	^{o}C	Ambient Storage Temperature


Analog Power and Ground
Digital Interface
J5
J4
S1
push button
P9
SPI Interface
Digital Power and Ground
U1
Apex_sm
J2
J3
GND split
Pwr split
Rauch Filters
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Main Section
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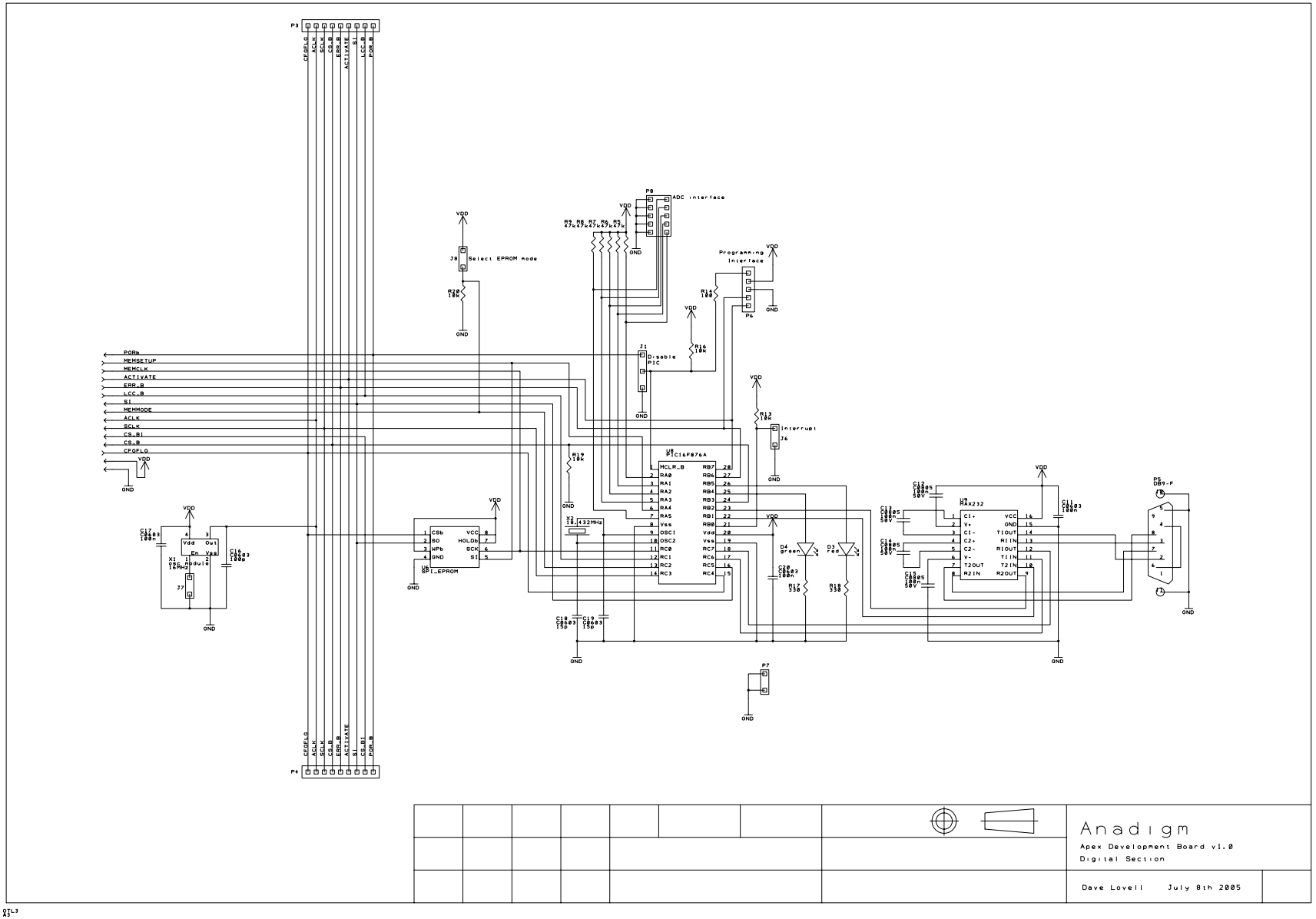
P3
P4
PORb
MEMSETUP
MEMCLK
ACTIVATE
ERR_B
LCC_B
SI
MEMMODE
ACLK
SCLK
CS_BI
CS_B
CFGFLG
VDD
GND
P8
ADC interface
J8
Select EPROM mode
R20
10k
Programming Interface
P6
R14
10k
J1
Disable PIC
R13
10k
Interrupt
J6
R12
10k
U6
PIC16F876A
MCLR_B
RA0
RA1
RA2
RA3
RA4
RA5
Vss
OSC1
OSC2
RC0
RC1
RC2
RC3
RB7
RB6
RB5
RB4
RB3
RB2
RB1
RB0
Vdd
RC7
RC6
RC5
RC4
X2
16.432MHz
U5
SPI_EPROM
CSb
SO
WPb
GND
VCC
HOLDb
SCK
SI
X1
12MHz
J7
C16
C17
C18
C19
C20
C21
C22
C23
U3
MAX232
C1+
V+
C1-
C2+
C2-
V-
T2OUT
R2IN
VCC
GND
T1OUT
R1IN
R1OUT
T1IN
T2IN
R2OUT
P5
DB9-F
D4
green
D3
red
R17
330
R18
330
P7
Anadigm
Apex Development Board v1.0
Digital Section
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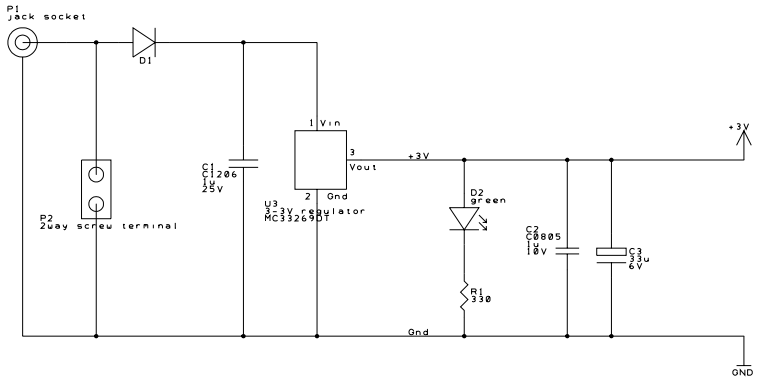
July 8th 2005



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								Power Section	
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OTL2
A4

Notes:

More Notes:

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