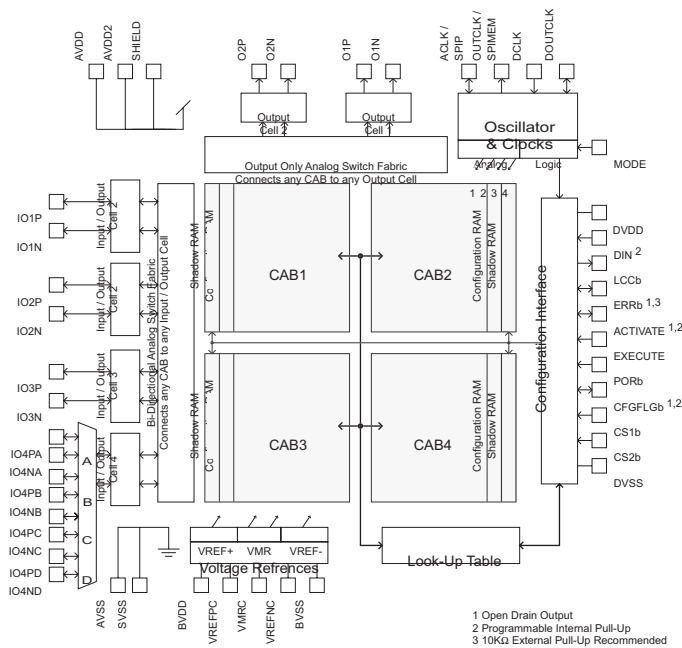


AnadigmVortex is the second generation field programmable analog array (FPAAs) device family from Anadigm. Nine members of the AnadigmVortex family are currently shipping providing a range of solutions to meet your analog signal processing requirements.

Static Configuration	Dynamically Reconfigurable	Input Cells	In/Out Cells	Output Cells	CABs	
AN120E04	AN220E04	4	-	2	4	Specialized input cell features
AN121E04	AN221E04	-	4	2	4	Bi-directional input/output cells

AN12x devices are best suited for are geared towards high-volume applications requiring consolidation of discrete analog functionality. The configuration interface of the AN22x devices is enhanced to accommodate dynamic reconfiguration - a breakthrough capability that allows analog functions to be integrated within the system and controlled by companion processor



AnadigmVortex devices consist of a 2x2 or 1x2 matrix of fully Configurable Analog Blocks (CABs), surrounded by a fabric of programmable interconnect resources. Fully differential signal paths ensure high fidelity operation. The second generation AnadigmVortex architecture provides a significantly improved signal-to-noise ratio as well as higher bandwidth.

These devices accommodate non-linear functions such as sensor response linearization and arbitrary waveform synthesis.

The ANx27 SonicMaster™ series is specially optimized for optimal performance through the audio band, providing never before possible audio system design options.

Some of the notable features of the Anadigmvortex solution include:

- Analog design time reduction from months to minutes
- Faster time-to-solution compared to discretely or ASIC
- High precision operation despite system degradation and aging
- Eliminating the need to source and maintain multiple inventories of product
- Ability to implement multiple chip configurations in a single device and to adapt functionality in the field

*The Anadigmvortex solution allows OEMs to deliver differentiated solutions faster and at lower overall system cost.*

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# 1 Architecture Overview

Anadigm offers the AN12x and the AN22x series Field Programmable Analog Array (FPAA) devices. The AN12x devices can be reprogrammed as many times as desired, however the device must first be reset before issuing another configuration data set. Once a Primary Configuration is complete; the configuration interface of the AN12x device ignores all further input. No further data writes are accepted unless a reset sequence is first completed. The AN22x devices are dynamically reconfigurable; the behavior of the FPAA can be modified partially or completely while operating.

Dynamic Reconfiguration available on the AN22x devices, allows the host processor to send new configuration data to the FPAA while the old configuration is active and running. Once the new data load is complete, the transfer to the new analog signal processing configuration happens in a single clock cycle. Dynamic Reconfiguration in the AN22x device allows the user to develop innovative analog systems that can be updated (fully or partially) in real-time.

The FPAA contains either 2 or 4 Configurable Analog Blocks (CABs) in its core. Most of the analog signal processing occurs within these CABs and is done with fully differential circuitry. The CABs have access to a single Look Up Table (LUT) which offers a method of adjusting any programmable element within the device in response to a signal or time base. It can be used to implement arbitrary input-to-output transfer functions (companding, sensor linearization), generate arbitrary signals, and construct voltage dependent filtering. A Voltage Reference Generator supplies reference voltages to each of the CABs within the device and has external pins for the connection of filtering capacitors.

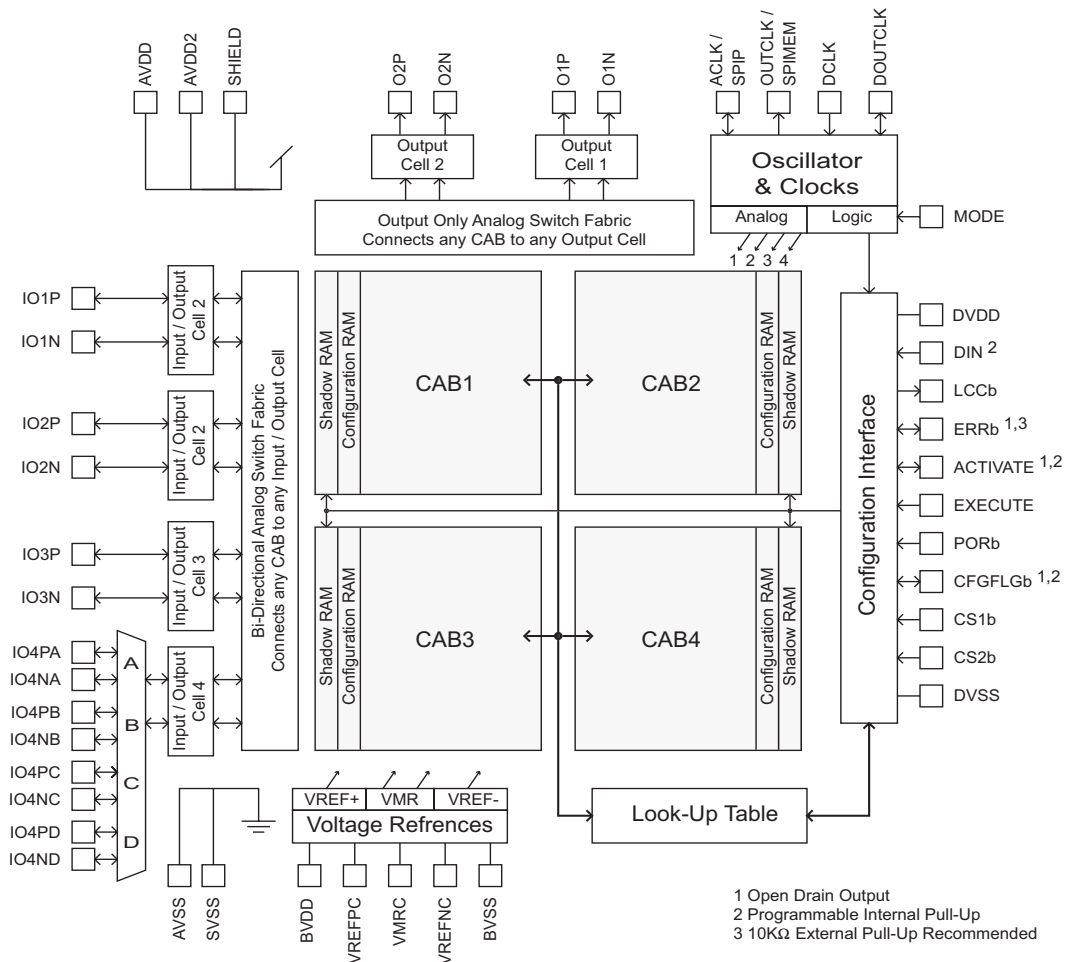


Figure 1 – Chip Overview for a Typical Four CAB AnadigmVortex FPAA

Analog inputs signals are routed into the FPAA core via any of the four Input Cells. The Input Cells can accept either differential pair or single-ended signals. The fourth Input Cell has a special front end multiplexer which allows for the connection of up to four differential pairs or eight single ended signals. ANx20 and ANx21 devices provide optional active signal processing elements in the Input Cells which provide programmable gain and anti-aliasing filtering. All the Input Cells also provide a direct input path to the FPAA core.

The ANx20 Input Cell provides only an input path; all other family members also provide a direct output path.

Analog output signals are routed out of the FPAA core via either of the two Output Cells or through the Input Cells direct output option. ANx20 and ANx21 devices provide optional active signal processing elements in the Output Cells which provide programmable gain and reconstruction filtering. The Output Cells also provide a digital output path used for comparator and SAR results data.

The FPAA can accept either an external clock or generate its own clock using an on chip oscillator and an external crystal. Detection of the crystal is automatic. The resulting internal clock frequency can be divided down into four synchronized internal switched capacitor clocks of different frequencies by programmable dividers. The clock circuitry can also source any of these four clocks as a chip output.

The behavior of the CABs, clocks, signal routing, Input Cells, and Output Cells, is controlled by the contents of Configuration SRAM. Behind every Configuration SRAM bit is a Shadow SRAM bit. The Shadow SRAM of the AN22x devices may be updated without disturbing the currently active analog processing. This allows for on-the-fly modification of one or more analog functions. This dynamic reconfiguration is not possible with the AN12x devices.

The architecture includes a highly flexible digital configuration interface. The configuration interface is designed to work in stand-alone mode by connecting to either a common SPI type serial EPROM. In this mode, after the device powers up, it will automatically load its configuration data from the EPROM and begin analog signal processing.

The configuration interface is also designed to be connected directly to a host microprocessor's SPI master port where it presents itself as a SPI compatible slave. The configuration interface also allows multiple devices to be easily connected together to build up larger analog processing systems.

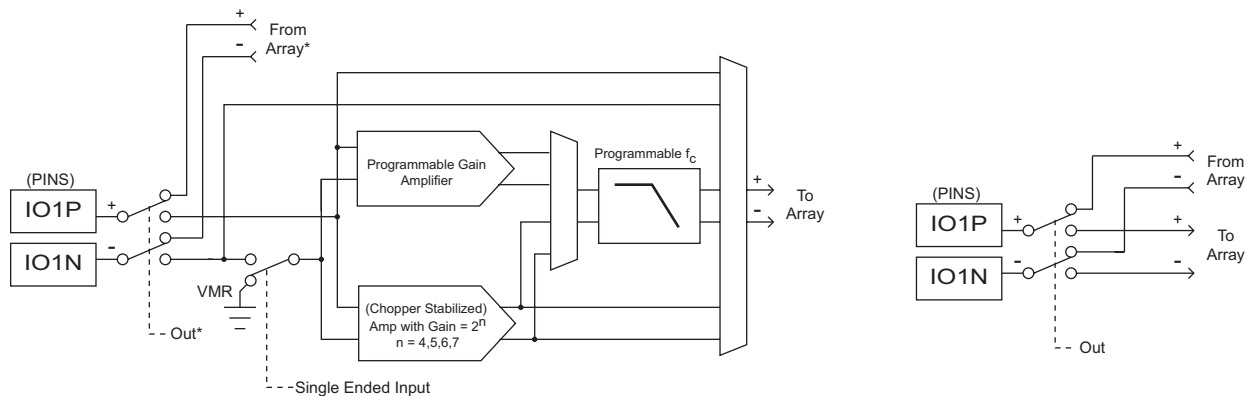
## 2 Analog Architecture Details

### 2.1 Input Cell

Each Input Cell contains a collection of resources which allow for high fidelity connections to and from the outside world with no need for additional external components. In order to maximize signal fidelity, all signal routing and processing within the device is fully differential. Accordingly each Input Cell accepts a differential signal.

Device Number	Unique Input Cell Features
ANx20	Input only. Chopper stabilized low offset input amplifier with programmable gain, Standard input amplifier with programmable gain, Programmable anti-aliasing input filter, Direct input
ANx21	Bidirectional. Chopper stabilized low offset input amplifier with programmable gain, Standard input amplifier with programmable gain, Programmable anti-aliasing input filter, Direct input, Direct output
ANx22	Bidirectional. Direct input, Direct output
ANx27	Bidirectional. Direct input, Direct output

A single ended signal can be used as an input to the cell. If a single ended source is attached, an internal switch will connect the negative side of the internal differential signal pair to Voltage Main Reference (VMR is the reference point for all internal signal processing and is set at 2.0 V above AVSS).



\* The output path is not available on the ANx20 devices.

Figure 2 – Fully Featured Input Cell for ANx20 & ANx21, and Simplified ANx22 & ANx27

As with any sampled data system, it may sometimes be necessary to low pass filter the incoming signal to prevent aliasing artifacts. The input path of the ANx20 and ANx21 Input Cell contains a second order programmable anti-aliasing filter. The filter may be bypassed, or set to selected corner frequencies.

When using the anti-aliasing filter, Anadigm recommends that the ratio of filter corner frequency to maximum signal frequency should be at least 30. These filters are a useful, integrated feature for low-frequency signals (signals with frequency up to 15kHz) only; and if high-order anti-aliasing is required. Where input signal frequencies are higher, Anadigm does recommend the use of external anti-aliasing.

A second unique input resource available within each ANx20 and ANx21 Input Cell is an amplifier with programmable gain and optional chopper stabilizing circuitry. The chopper stabilized amplifier greatly reduces the input offset voltage normally associated with op-amps. This can be very useful for applications where the incoming signal is very weak and requires a high gain amplifier at the input. The programmable gain of the amplifier can be set to  $2^n$  where  $n = 4$  through 7. The output of the amplifier can be routed through the programmable anti-aliasing input filter, or directly into the CABs. Single-ended input signals must use either the amplifier or the anti-alias filter in order to get the required single to differential conversion. The programmable gain amplifier, the chopper stabilized amplifier and the programmable anti-aliasing filter are all resources available only on the input signal path.

When the Input Cell is used as a bypass mode input or as an output, the connection is direct and unbuffered. There are no active circuit elements available in the Input Cell when it is configured for either input or output bypass.

ANx22 and ANx27 devices have streamlined Input Cells. These devices offer only the direct unbuffered signal paths into and out of the CABs.

### 2.1.1 Special Consideration for Bypass Outputs

When using either an Output Cell or an Input Cell in bypass output mode, special care must be taken to not overload the device. In bypass mode, there are no buffers between the CAB's signal source and the device's output pins.

The CAB op-amps are not designed to drive low impedances. Also, too much load capacitance will destabilize the CAB op-amps. The minimum recommended external load resistance should be not less than 100 K $\Omega$  and the maximum external load capacitance should be not more than 100 pF. When using bypass mode outputs, characterization of the final system is essential.

## 2.2 Muxed Analog Input / Output

There is a bi-directional multiplexer available in front of one of the Input Cells. This allows the physical connection of 8 single ended inputs, 4 differential pair inputs, or 4 differential pair output loads at once, though only one source or load at a time can be processed by the FPAAs. As with the regular Input Cells, the optimal input connection is from a differential signal source. If a single ended connection is programmed, the negative side of the internal differential pair will be connected to Voltage Main Reference.

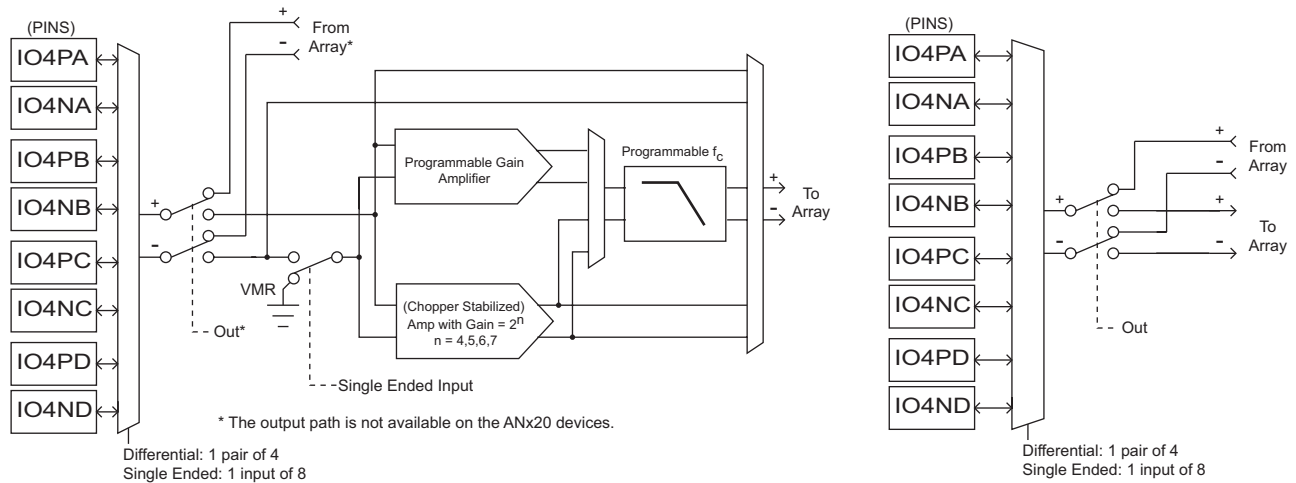


Figure 3 – Fully Featured Muxed Input Cell for ANx20 & ANx21, and Simplified ANx22 & ANx27

## 2.3 Output Cell

Like the Input Cells, the Output Cells are designed to ensure that your system's design can take full advantage of the fidelity and versatility that the core of the device offers. The outputs can serve to deliver digital data, or differential analog voltage signals.

Device Number	Unique Output Cell Features
ANx20	Direct Output, Unity Gain Buffer with Programmable Gain Reconstruction Filter
ANx21	Direct Output, Unity Gain Buffer with Programmable Gain Reconstruction Filter, Digital Output (SAR and Comparator)
ANx22	Direct output
ANx27	Direct output

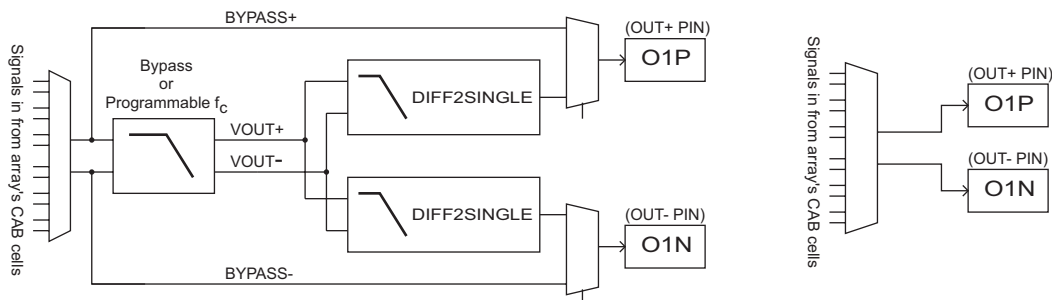


Figure 4 – Fully Featured Output Cell for ANx20 & ANx21, and Simplified ANx22 & ANx27

Analog signal pairs sourced by CABs within the array are routed to an Output Cell via the Output Cell's input multiplexer.

It may be desirable to route the core analog signals to the outside world with no additional buffering or filtering. The ANx20 and ANx21 Output Cells have bypass paths which allow the core signals to come out with no further processing or buffering. For special considerations governing the use of bypass mode outputs, see Section 2.1.1.

The ANx20 and ANx21 Output Cells contain a programmable filter identical to the one described for the Input Cells (see Section 2.1). The filter may be bypassed, or set to selected corner frequencies. Whereas the filter structure served as an anti-aliasing filter for the input, in the Output Cell it serves as a 2<sup>nd</sup> order reconstruction filter. In this function, it smooths out the sampling induced stair step nature of the output waveform.

A differential to single converter circuit follows the programmable filter. After the programmable filter and the DIFF2SINGLE conversion, the system designer may elect to utilize only one of the OUT signals, referencing it to Voltage Main Reference (VMR), or use them both (OUT+ and OUT-) as a differential pair. Remember that a single-ended output will have half the amplitude of a differential signal.

ANx22 and ANx27 devices have streamlined Output Cells. These devices offer only the direct unbuffered signal paths out of the CABs.

## 2.4 Configurable Analog Block

Within the FPAA, there are two (AN221E02) or four (all other family members) Configurable Analog Blocks (CABs). The functions available in the CAM library are mapped on to these programmable analog circuits. Figure 5 shows an overview of the Configurable Analog Block (CAB).

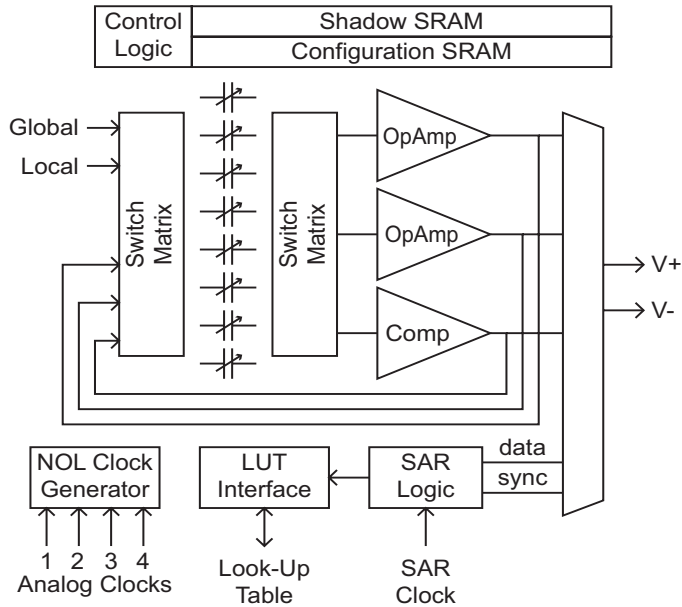


Figure 5 – Overview of a Configurable Analog Block

Among the many analog switches within the CAB, some are static and determine things like the general CAB circuit connections, capacitor values, and which input is active. Other switches are dynamic and can change under control of the analog input signal, the phase of the clock selected, and the SAR logic. Whether static or dynamic, all of the switches are controlled by the Configuration SRAM.

As part of the power-on reset sequence, SRAM is cleared to a known (safe) state. It is the job of the configuration logic to transfer data from the outside world into the Shadow SRAM and from there, copy it into the Configuration SRAM. The AN22x devices allow reconfiguration. While an AN22x device is operating, the Shadow SRAM can be reloaded with values that will sometime later be used to update the Configuration SRAM. In this fashion, the FPAA can be reprogrammed on-the-fly, accomplishing anything from minor changes in circuit characteristics to complete functional context switches, instantaneously and without interrupting the signal path. The AN12x devices must be reset between complete configuration loads and do not accept partial reconfigurations.

Analog signals route in from the cell's nearest neighbors using local routing resources. These input signals connect up to a first bank of analog switches. Feedback from the CAB's two internal op-amps and single comparator also route back into this input switch matrix.

Next is a bank of 8 programmable capacitors. Each of these 8 capacitors is actually a large bank of small but equally sized capacitors. Each of these 8 programmable capacitors can take on a relative value between 0 and 255 units of capacitance. The actual value of capacitance is not all that important here. The CAM library elements do not depend on the absolute value of these capacitors, but rather on the ratio between them, which tracks to better than an 0.1%.

There is a second switch matrix used to complete the circuit topology by making the appropriate connections. There are two op-amps and a single comparator at the heart of the CAB. Outputs of these active devices are

routed back into the first switch matrix so feedback circuits can be constructed. These outputs also go to neighboring CABs.

Signal processing within the CAB is usually handled with a switched capacitor circuit. Switched capacitor circuits need non-overlapping (NOL) clocks in order to function correctly. The NOL Clock Generator portion of the CAB takes one of the four available analog clocks and generates all the non-overlapping clocks the CAB requires.

There is Successive Approximation Register (SAR) logic that, when enabled, uses the comparator within the CAB to implement an 8 bit analog converter. Routing the SAR's output back into its own CAB or to the Look Up Table enables the creation of non-linear analog functions like voltage multiplication, companding, linearization and automatic gain control.

## 2.5 Look Up Table

The device contains a single 256 byte Look Up Table (LUT). The 8 bit address input to the LUT can come from either the a SAR 8 bit output or from a special 8 bit LUT counter. The functional description of the SAR driving the LUT address inputs is given in the section below.

If the LUT counter is selected, the counter continuously counts up, resetting itself back to zero count each time that its programmable roll-over value is met. Each new count value is presented to the LUT as an address. The data read back from this address is then written into 1 or 2 target locations within Shadow SRAM. The target location(s) to be used and LUT contents are part of the device's configuration data set. The clock to the LUT counter is sourced by one of the 4 internal analog clocks (from one of the four clock dividers).

The subsequent transfer of these 1 or 2 bytes from Shadow SRAM into Configuration SRAM can occur as soon as the last configuration data byte is sent, or an internal zero crossing is detected, or a comparator trip point is met, or an external EXECUTE signal is detected.

With periodic clocking of the LUT counter, a LUT / CAB combination can form an arbitrary waveform generator, or temporally modulate a signal.

## 2.6 SAR Operation

Circuitry is included within the CAB which allows the construction of an 8-bit Successive Approximation Register (SAR) type analog converter. The SAR requires two clocks with a frequency ratio of 16 to 1. The slower clock (SAR clock, a.k.a. CLOCKA) determines the rate at which successive conversions will occur and should not exceed 250 KHz. The faster clock (SC clock, a.k.a. CLOCKB) is used to do the conversion itself. These clocks are generated by the normal clock divider circuitry.

The SAR result is in the sign magnitude format (1 bit sign, 7 bits magnitude). The SAR inputs should be limited to  $V_{MR} \pm 1.5 V$ . Inputs going above  $V_{REFPC}$  ( $V_{MR} + 1.5 V$ ) and below  $V_{REFMC}$  ( $V_{MR} - 1.5 V$ ) will result in the output railing to either 7F or FF as appropriate.

The SAR result can be routed to either the LUT's address port or back into its host CAB. The most common use of the SAR is to serve as an address generator for the Look Up Table. At the end of every conversion, the 8 bit result is recognized by the LUT as a new address. The configuration circuitry takes the LUT contents pointed to by this address and loads it into one or two specific locations in the Shadow SRAM.

A typical use scenario is where an input signal needs to be linearized and or calibrated. A signal comes in from the outside world and is presented to the CAB configured to do a SAR conversion. The SAR result is routed to the LUT where a linearization table was stored as part of the device's configuration image. Using the same mechanism as described for the LUT counter in section 2.5, the configuration circuitry takes the LUT contents pointed to by this address (the SAR result byte) and loads it into 1 or 2 specific Shadow SRAM locations. For this example, these locations would likely adjust the gain of an amplifier, thus achieving the desired























































