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Introduction

The Anadigmvortex family of FPAA's uses analog signals that are referenced to +2 V (VMR) and are limited to the range 0 to +4 V. This application note describes a number of methods for interfacing these FPAA's to signals that are biased at voltages other than +2 V and/or whose amplitude exceeds the range 0 to +4 V.

The list of methods is not exhaustive and is provided only as a guide. The reader may wish to mix and match aspects from different methods or combine them with others not listed.

Single-Ended Operation

Before discussing the different methods of interfacing analog signals to the FPAA, it is important to realize that the device can be used in single-ended or differential mode. Figure 1 illustrates how to interface single-ended signals to the FPAA.

The input should be set in single-ended mode. To do this requires also setting the low pass anti-alias filter which has a maximum corner frequency of 470 kHz. It can also be done by setting the amplifier or the low offset chopper amplifier, but these have a minimum gain of 16 which may not be required. If the signal frequency is greater than 470 kHz and a gain of 16 cannot be tolerated then the input cannot be used in single-ended mode. In this case the negative input should be connected to +2 V (VMR) externally.

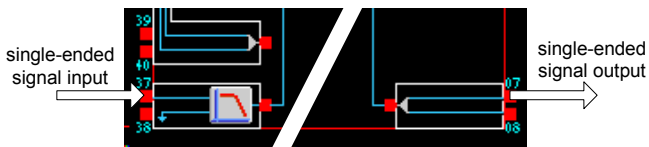


Figure 1. FPAA in Single-Ended Mode

The output of the FPAA can also be used in single-ended mode simply by connecting to only one of the differential pair (see Figure 1). The positive or negative output can be used (the negative output will be inverted).

Method 1: D.C. Biased Input

If the input signal to the FPAA is single-ended and has a small unwanted d.c. bias but remains within the range 0 to +4 V, then it is possible to effectively remove this bias by applying an appropriate d.c. bias to the negative input of the differential pair. To do this requires that the input is not set in single-ended mode. Figure 2 shows an example of a +2.5 V referenced, single-ended signal connected to the positive input and a +2.5 V d.c. bias connected to the negative input.

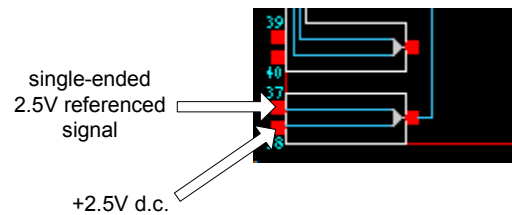


Figure 2. D.C. Biased Input

This method has the advantage of being very simple. Its disadvantages are that it only works with single-ended signals, and only works for the input of the FPAA (the output cannot be level-shifted in a similar manner). Additionally, the input signal with its d.c. bias must be within the 0 to +4 V range.

Method 2: CAMs

If the input signal to the FPAA has a small unwanted d.c. bias but remains within the 0 to +4 V range, then it is possible to use a high-pass filter within the FPAA to remove the bias (see Figure 3). An example might be a signal whose amplitude is 2 V peak to peak and is referenced to +2.5 V. For a differential signal this is a common mode d.c. bias, but it may also have a differential d.c. bias. The high-pass filter will remove both common mode and differential biases.

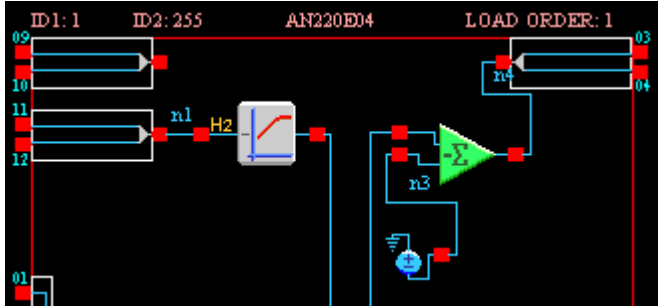


Figure 3. CAMs for Control of d.c. Bias

Note 1: The corner frequency of the filter must be set well below the working frequency range of the input signal.

Note 2: The filter has a gain setting which allows input signals to be amplified up to a gain of 20 (amplification using a high pass filter has the advantage that not only are d.c. biases on the input signal ignored but so are amplifier offsets from within the CAM). The gain setting can also be used to attenuate the incoming signal, but this cannot be used to attenuate signals exceeding the 0 to +4 V input range. Such signals will be clipped, regardless of being attenuated.

If the signal out of the FPAA needs to be level-shifted e.g. it may be required to drive a device referenced to 2.5 V, then it should be understood that there is no means of shifting the common mode d.c. bias of the differential output of the FPAA using CAMs. However, if the output is being used in single-ended mode i.e. only the Oxp or OxN pin is used, then the d.c. bias can be shifted by using a SumInv CAM with a Voltage Source connected to its second input (see Figure 3).

Note 1: The Voltage Source is fixed at +/-3V so to shift the d.c. bias of the single-ended signal by 0.5 V (from +2 to +2.5 V) requires setting the gain on the lower input of the SumInv CAM to 1/3 (the level shift of the single-ended output is half that of the differential output).

Note 2: The Voltage Source in Figure 3 is set to negative (-3 V). This leads to a positive level shift on the Oxp output pin because the SumInv CAM is inverting. As with the input, the output signal must be confined to the range 0 to +4 V.

This method has the advantage of being inexpensive since no external components are required. Its disadvantages are: DC information is lost from the input signal, it uses FPAA resources, the method for level-shifting the output only works with single-ended signals, and both input and output signals are confined to the 0 to +4 V range.

Method 3: A.C. Coupling

Another method of dealing with unwanted d.c. bias on the input signal is to a.c. couple it (see Figure 4). If no attenuation of the input signal is required then in most cases R and Ra are not needed (top input in Figure 4). This is because most CAMs pull the inputs to VMR (+2 V). In certain circumstances this is not true (see Note 1), in which case R must be used to pull the input to VMR (middle input in Figure 4).

The values of R and C should be as high as possible to give a cut-off frequency well below the working range of the input signal. The cut-off frequency can be calculated from the values of R and C with the formula:

$$F_c = 1 / (2 * \pi * R * C)$$

If R is not used because the first CAM is pulling the inputs to +2 V (see Note 1) then the cut-off frequency can be calculated based on the equivalent resistance of 30kΩ between the CAM input and VMR e.g. a value of C = 0.1 uF will give a cut-off frequency of about 50 Hz.

If it is necessary to attenuate the incoming signal, then both R and Ra are needed (bottom input in Figure 4). The values of R and Ra should be chosen to achieve the required amount of attenuation, however it should be understood that most CAMs pull the inputs to VMR with an equivalent resistance of about 30kΩ (see Note 1 below). For this reason R should be kept well below 30 kΩ to achieve an accurate attenuation e.g. to attenuate the input signal by 0.1, appropriate values might be R = 1 kΩ and Ra = 9 kΩ.

Figure 4 shows single-ended operation but the circuit can be doubled up for differential operation, i.e. put the R and C on each pin of the differential pair.

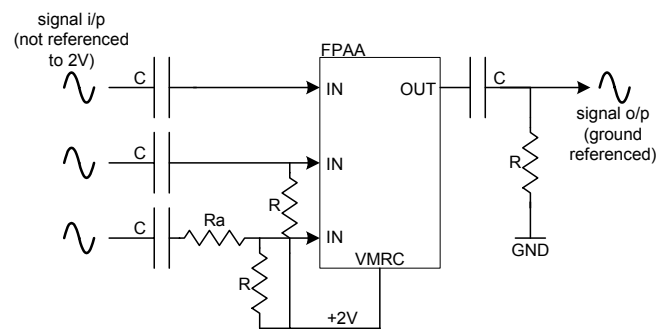


Figure 4. A.C. Coupling

Note 1: In many cases the resistor R is not required because most CAMs pull their inputs to VMR (+2 V) with an equivalent resistance of about 30 kΩ at a clock frequency of 4MHz (this resistance varies inversely

with clock frequency). Exceptions are: if the first CAM in the FPAA is a high pass filter (Bilinear or Biquad), a Differentiator, a Comparator, a Hold or a RectifierHold. Also, if the input is in 'low-pass filter' mode, 'low offset chopper' mode, or 'amplifier' mode then the inputs will not pull to VMR, regardless of which is the first CAM.

Note 2: If the FPAA has not had a primary configuration then the VMRC pin will not be outputting +2 V (it will be tristate).

The output from the FPAA can also be a.c. coupled in order to shift it to another reference level. Figure 4 shows the output signal being converted to a ground referenced signal. Again the values of R and C should be set to give a corner frequency well below the working range of the output signal (in many cases these will be the same values as used on the input).

The main advantages: It is inexpensive, does not require components with tight tolerances, can cope with signals that have any amount of d.c. bias, and can cope with input signals of any amplitude. It has the disadvantage that DC information in the signal is lost.

Method 4: Chopper Amplifier

This method is concerned only with differential signals on the input which have a floating reference and a small amplitude. The reason for devoting a section to such a particular class of signals is that they are quite common - examples being microphones and thermocouples.

This type of signal source should be connected directly to the FPAA input which should be set in 'low offset chopper' mode. The chopper amplifier amplifies the input signal by a factor in the range 16 to 128 in steps of 16, without adding any unwanted offsets to the signal. Since the chopper amplifier does not pull its inputs to +2 V, a pair of resistors between the differential inputs and the VMRC pin is needed (see Figure 5). These resistors should be significantly larger than the source impedance of the signal (which tends to be high for this class of signal).

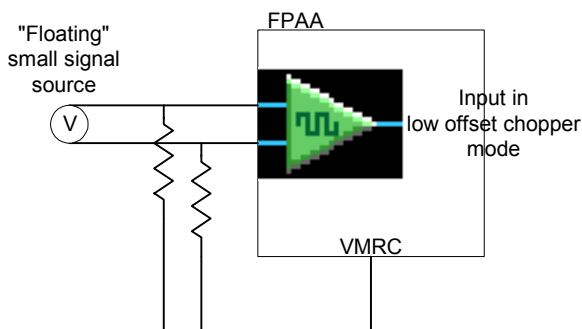


Figure 5. Chopper Amplifier

This method has the advantage of being cheap and simple with no dependence on component tolerances. Its disadvantage is that it can only be used with low amplitude floating signals.

Method 5: Resistor Dividers

Another simple method of level-shifting signals with unwanted d.c. biases is to use resistor dividers. Figure 6 shows an implementation of this method for using ground referenced signals both into and out of the FPAA. It shows single-ended operation but the circuit can be doubled up for differential operation. The resistor values have to be chosen to shift the signal into the FPAA to +2 V and the signal out of the FPAA to whatever the next stage requires (ground in this case).

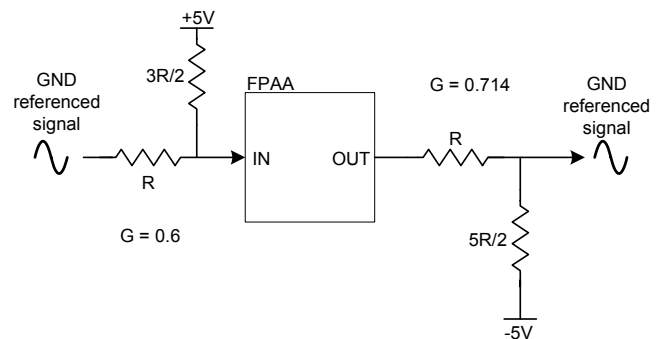


Figure 6. Resistor Dividers

Note 1: The divider on the input is connected to +5 V which means that it can only level-shift up (from ground to +2 V in this case). If the divider needs to level-shift down (e.g. +2.5 V to +2 V) then it needs to be connected to ground or -5 V (connecting to ground removes dependence on supply tolerance). Similarly, the divider on the output is connected to -5 V so can only level-shift down (+2 V to ground in this case). To level-shift up (e.g. +2 V to +2.5 V) requires it to be connected to +5 V.

Note 2: Using a resistor divider on the output may be unsuitable if the next stage has a low input impedance. The resistor values in the divider need to be significantly lower than the input impedance of the device they are driving, but they cannot be too low as to overload the FPAA output. It is not recommended to make the sum of the resistors in the output divider less than 100 kΩ.

Note 3: Both the dividers attenuate the signal. In the case of the circuit in Figure 6, the signal is attenuated by a factor of 0.6 on the input and 0.714 on the output. As far as the input is concerned, this attenuation may be an advantage if the signal's amplitude exceeds 4 V

p.p. (8 V p.p. differential). The amount of attenuation cannot be chosen by the user since it is fixed by the level-shifting requirement (0 V to +2 V in Figure 6) unless a third resistor is introduced. Figure 7 shows a 3 resistor divider designed to level-shift the input signal from 0 V to +2 V and attenuate it by a factor of 0.1.

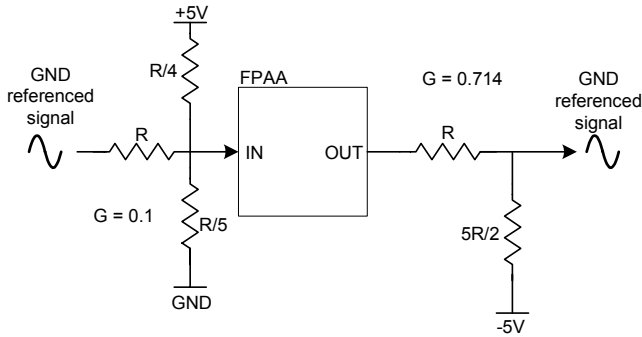


Figure 7. 3-Resistor Divider

The advantages of this method are it is inexpensive, it has the ability to handle large signals on the input, to handle signals of any d.c. bias, and it transmits DC. The disadvantages are that the output signal is attenuated, and the amount by which both input and output signals are attenuated and level-shifted depends on resistor and supply tolerances. Also, using a resistor divider on the FPAA output may not be suitable if the next stage has a low input impedance.

Method 6: Zener Diodes

This method uses zener diodes and resistors to carry out the level shifting. It overcomes nearly all of the disadvantages of the previous method since it does not depend on resistor or supply tolerances and there is no attenuation of the output signal. Figure 8 shows an example of using 2 V zener diodes to interface the FPAA to ground referenced signals. It shows single-ended operation but the circuit can be doubled up for differential operation.

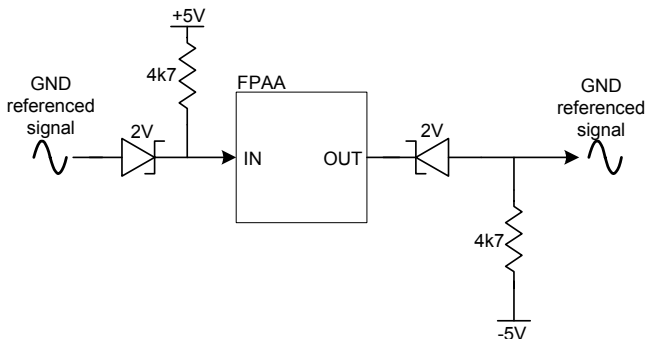


Figure 8. Zener Diodes

The advantages of this method are its relative inexpensiveness, lack of dependence on resistor or supply tolerances, lack of attenuation on the output and its ability to cope with signals referenced to any voltage (provided the appropriate zener diodes can be found). Its disadvantages are its dependence on the zener tolerances, and that the gain is fixed at 1 so it cannot handle signals with amplitude greater than 4 V p.p. (8 V p.p. differential).

Method 7: Reference VMR to Ground

This method allows the FPAA to be used directly with ground referenced signals. The way this is done is by connecting the ground of the system external to the FPAA (system ground) to +2 V with respect to the FPAA's supply (FPAA VMR). This cannot be done by connecting system ground to the VMRC pin of the FPAA because the VMRC pin does not output +2 V until the FPAA has received a primary configuration, before this it is tristate. The reason this is a problem is that the configuration clock and data will come from the system, so to perform a primary configuration, the FPAA and system supplies must already be tied (referenced to each other). The digital interface between the FPAA and system is discussed later.

Figure 9 shows the relationship between the voltages of the FPAA and system. The FPAA's supply is generated by a +5 V regulator and VMR by a +2 V regulator. VMR is connected directly to system ground and the system's dual supply is generated from a +5 V regulator and a DC-DC voltage converter to generate the -5 V. The system will contain both digital circuitry for configuring the FPAA and analog circuitry for the processing of ground referenced signals.

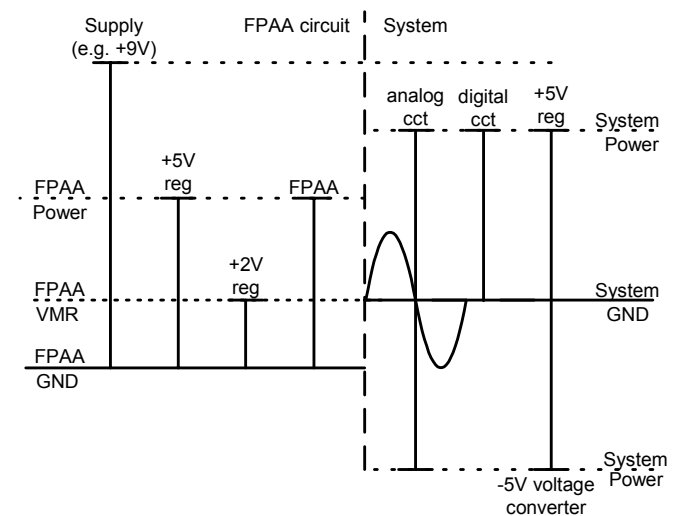


Figure 9. Connect VMR to GND v1

Note 1: If system ground is connected to earth ground then it is important that the supply (+9 V in Figure 9) is isolated from earth ground, e.g. battery or wall transformer. Conversely, if the supply is ground referenced then the system ground must be isolated from earth ground.

Note 2: Voltage converters use a charge-pump which uses an internally generated clock. This clock can create a small amount of interference so it is recommended to provide plenty of decoupling on the -5 V supply.

An alternative version of this method is shown in Figure 10. In this case the system is powered by a dual supply and the FPAA supply is generated using +3 V regulators referenced to -5 V and system ground. The weakness in this approach is that it makes VMR depend on both the regulator's tolerance and that of the negative supply. It would be preferable to generate the FPAA's ground using a -2 V regulator referenced to system ground. Unfortunately, -2 V regulators are difficult to find.

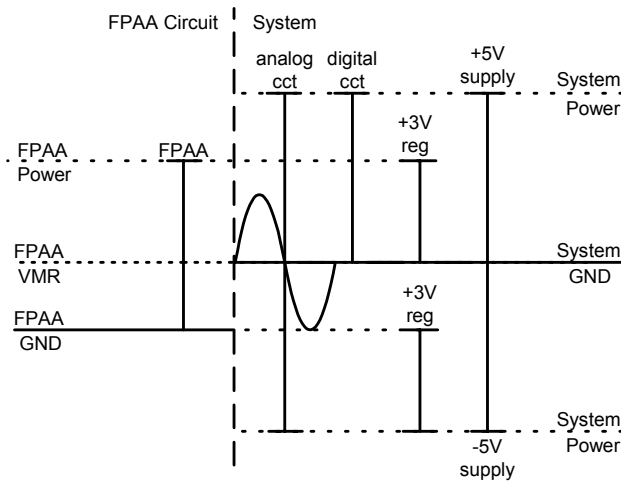


Figure 10. Connect VMR to GND v2

These methods require interfacing digital signals between the digital circuit and the FPAA. This is necessary to configure the FPAA. Figure 11 shows how this can be achieved using 2 V zener diodes.

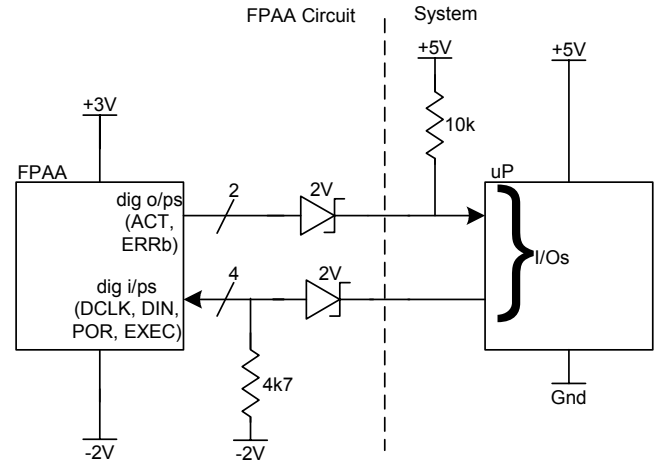


Figure 11. Digital Level-Shifting

Note: Although there are six digital signals shown in Figure 11, configuration can be achieved with just DCLK and DIN (the minimum requirement).

This method has the advantage that no level shifting of the analog signals is required and a simple potential divider to (system) ground can be used to attenuate large signals on the input. The disadvantages are that it is more expensive due to the regulators and it requires extra components to interface the digital signals.

Method 8: Opamp Circuits

This method uses opamp circuits. Figure 12 shows how a ground referenced signal can be level-shifted to +2 V for input to the FPAA. This circuit can also be used to attenuate large signals or amplify small signals. The gain of the circuit is given by:

$$\text{Gain} = R_f / R_i$$

Figure 12 shows single-ended operation but the circuit can be doubled up for differential operation.

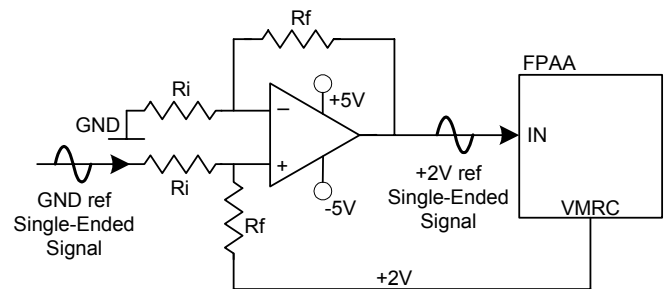


Figure 12. Level-Shift on the Input

Note: The VMRC pin must not be too heavily loaded. It is recommended to keep the sum of R_f and R_i to approximately 100 k Ω .

Figure 13 shows how a single opamp can be used to not only level-shift the FPAA output but also do a differential to single-ended conversion. Furthermore, this circuit can drive devices with low input impedance and can be used to amplify the FPAA output by any desired amount. The gain of this circuit is given by:

$$\text{Gain} = R_f / R_i$$

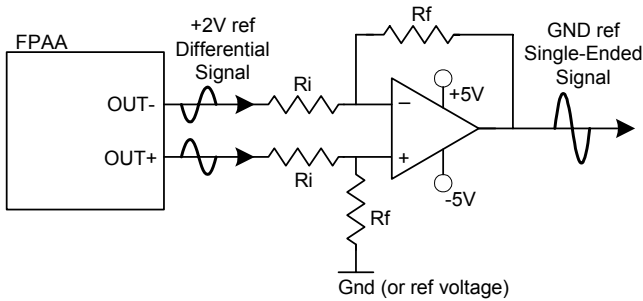


Figure 13. Level-Shift & Diff2Single on the Output

Note: The circuit in Figure 13 shows level shifting of the FPAA output to ground and it is the resistor R_f connected to ground that provides the reference for the level-shifted signal. However, this circuit can be used to level-shift the FPAA output to any desired voltage simply by connecting the resistor R_f to that voltage instead of ground.

The advantages of this method are that d.c. information is not lost, signals of any amplitude or d.c. bias can be handled, and the output can drive devices with low input impedance. Also the FPAA output can be both level-shifted and converted from differential to single-ended. The disadvantages are its dependence on resistor tolerances and its cost.

Method 9: Differential Opamps

This method uses differential opamps with common mode/reference voltage inputs. The AD8132 is an opamp with differential in and differential out pins and a common mode input. This device can be used to level-shift and/or perform single-ended to differential conversion. Figure 14 shows the basic circuit for a gain of 1. The input to this circuit can be differential or single-ended (lower input connected to ground). For more details on using this circuit, see the AD8132 data sheet available on the Analog Devices web page.

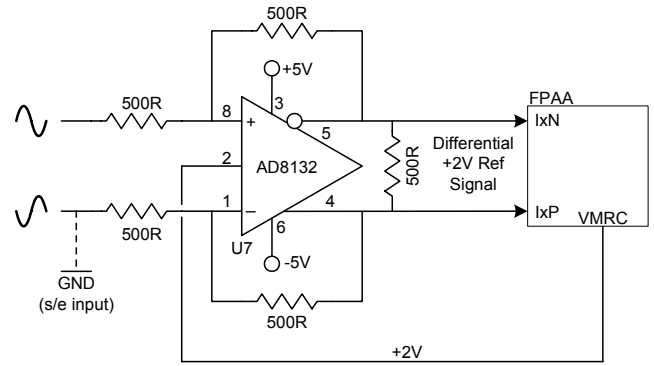


Figure 14. Single-to-differential Converter

Note 1: The AD8132 has very high bandwidth (350MHz) which may cause problems due to aliasing of high frequency noise. This can be avoided by connecting capacitors in parallel with the feedback resistors. For example, 1 nF capacitors will give a corner frequency of approximately 300 kHz.

Note 2: The resistor values in Figure 14 can be altered to change the gain of the circuit. This means that large amplitude signals can be attenuated before being input to the FPAA (this does not require that the AD8132's power supply has to encompass the voltage swing of the input signal because the attenuation is performed by the resistor dividers). The gain equals the ratio of feedback resistor to input resistor e.g. if a gain of 0.1 is required then the input resistors could be changed to 5 k Ω .

Note 3: Whether using the circuit in Figure 14 in single-ended or differential mode, it should be understood that the source impedance of the input signal will have the effect of reducing the gain of this circuit. For example, a source impedance of 50 Ω will have the effect of reducing the gain by about 10% in Figure 14. This can be compensated for by reducing the values of the input resistors (in single-ended mode, only reduce the value of the resistor connected to the signal, not the one connected to ground). In the case of Figure 14, the input resistor(s) should be reduced to 450 Ω for a 50 Ω source impedance.

Note 4: When connecting the VMRC pin of the FPAA to the common mode input, it should be understood that the level-shifting will not work until the FPAA is configured (VMRC is tristate until a primary configuration has taken place).

Figure 15 shows a differential to single-ended converter and level-shifter circuit. It uses the AD8132 which is a differential in single-ended out opamp with a reference voltage input. The gain of this circuit can be

altered by adjusting the values of the resistors. The gain is given by the formula:

$$\text{Gain} = 1 + (R_f / R_g)$$

For unity gain, connect pin 5 directly to pin 6 (no resistors required). For more details on using this circuit, see the AD8130 data sheet available on the Analog Devices web page.

any voltage, signals of any amplitude, and differential or single-ended signals. Its disadvantages are cost and the dependence of gains on resistor tolerances (except when using the AD8130 with gain = 1)

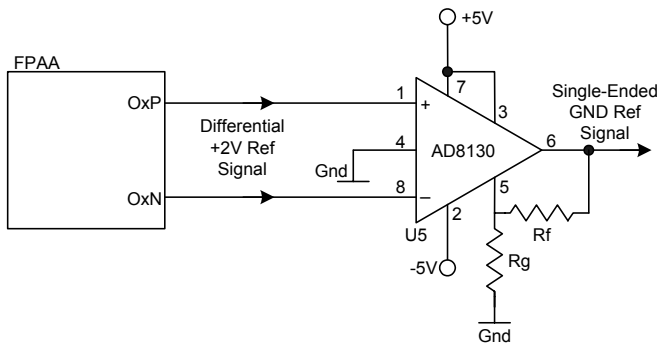


Figure 15. Differential-to-single Converter

Note 1: Figure 15 shows the FPAA output being level-shifted to ground, but the signal can be level-shifted to any voltage by connecting that voltage to the reference input (pin 4 of the AD8130 device). However, it must be understood that the level-shifted output signal of the AD8130 must be encompassed by its supply voltages with a margin of at least 1 V. So for example, if the output of the AD8130 needs to be referenced to +5 V with an amplitude of 4 V p.p., then the AD8130 must have a positive supply of at least +8 V. The AD8130 has a range of supply voltages up to +/-12.6 V.

Note 2: If this circuit is to be used to amplify the FPAA output by the addition of the two resistors Rf and Rg, then it should be understood that the output of the AD8130 must be encompassed by its supply voltages with a margin of at least 1 V. The maximum supply of the AD8130 is +/-12.6 V, so for example, the AD8130 can output ground referenced signals of up to about 23 V p.p. amplitude when using the maximum supply.

Note 3: The AD8130 has the limitation that it will clip differential signals on its inputs of amplitude greater than +/-2.8 V (the FPAA can output differential signals of up to +/-4 V amplitude).

Note 4: The AD8130 has a very high bandwidth (270MHz) which may be an advantage if the output from the FPAA is required to be half cycle e.g. if the last CAM in the FPAA circuit is a GainHalf CAM.

This method of using differential amplifiers has the advantages that it can handle signals referenced to