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# Wireless

## Design & Development

### Universal Baseband Signal Processing for RFID Readers

A cleaner signal from an analog filter means that the subsequent digital processing is much simpler.

By Simon Dickinson

There are two approaches to architectural design when considering a universal baseband signal processing for an RFID reader the: 1) “do it all in DSP method” or 2) dynamically programmable analog signal processing.

A universal baseband signal processor has to be capable of providing both gain and filtering multiple baseband signal frequencies. The majority of RFID tags used today employ a pseudo FSK signal protocol.

To add to the challenge of extracting a sub-carrier signal and decoding the information it conveys is the ever-increasing target read ranges and the low-cost passive

tags. A passive tag has no battery and no real means of being a radio transmitter.

RF and HF radio design is well known and understood. RFID tags and the associated reader bring a slightly different challenge to the RFID reader-radio designer. The “tag” end of the radio link is a passive device. It cannot “transmit” in the traditional sense as a radio. The response from a tag is “backscattered”. What the tag actually does is to extract and rectify a little power from the system carrier frequency (enough to power itself for a short time) then, when appropriate, it can turn on a transistor which effectively shorts its own antenna. The RF coupling between reader and tag will see this shorting of the tag antenna as a very small amplitude modulation.

Considering the “backscatter” signaling a little further, sub-carrier encode is realized using two distinct sub-carrier frequencies (see Figure 1). A carrier wave is amplitude modulated, using two different sub-carrier frequencies.

In simple terms, the receive channel electronic must demodulate the signal to remove the carrier frequency, then filter and apply gain to the remaining sub-carriers in order to extract two distinct frequencies (or time periods). These two different time periods correspond to logic “1” and “0”.

When considering standards, including EPC Global Gen 1/Gen 2 (Class 0, 1, 2) and ISO 18000-

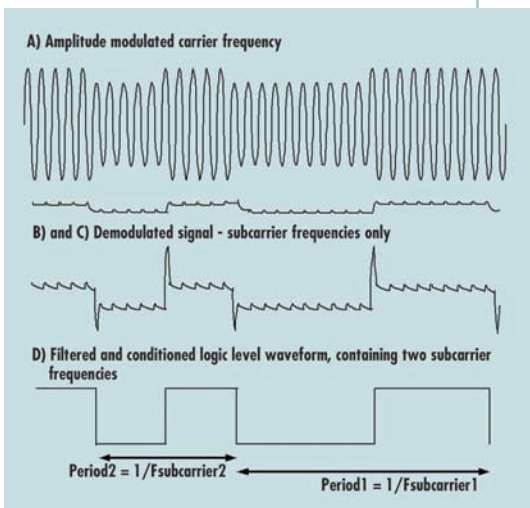


Figure 1.

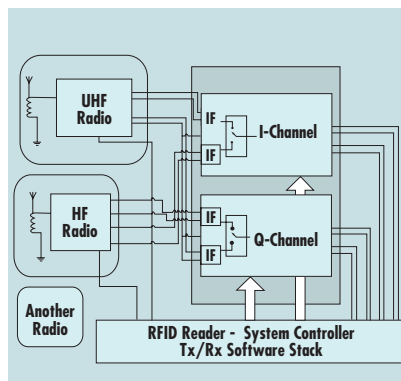


Figure 2.

6, 14443, 15693, the range of FSK sub-carrier frequencies varies from frequency pairs of 2 and 4 kHz to pair of 320 and 640 kHz; and there is the legacy of “class0” tags which has not completely disappeared.

If a universal baseband signal processor is to be used, a bandpass filter which covers 500 Hz to almost 1 MHz will be required. Such a wide filter will obviously also pass a huge amount of unwanted energy or noise. It is therefore more effective to construct a variable filter which can be focused to specific expected frequencies to limit the introduction of noise. “Do it all in DSP method” is modern, fashionable and, if you have or can find the DSP coding expertise and experience and have the engineering bandwidth to undertake such a task, an effective method for producing a baseband filter and extracting a very small signal from an equally sized noise floor.

In producing such a solution, the designer must consider a suitable ADC. For high performance RFID reader units this most likely needs to be differential and it needs to be fast. The highest baseband signal frequency from an EPC global gen2 tag is 640 kHz. To catch the 5th harmonic of this, an effective bandwidth of 3.2 MHz is needed. If the universal baseband signal-processing unit is also to process information from “class0” tags, the highest sub-carrier frequency is 3.3 MHz. In this case, it needs to be much faster. The ADC will, of course, capture all of the undesirable noise and other frequencies which are present at its inputs — a worse case scenario: “grab and digitize it all” and sort it out later with additional processing.

Given the wide variation in possible sub-carrier frequencies, a DSP filter architecture which is variable would be needed for optimum performance. Latency issues will limit the speed with which a filter can be changed effectively.

We also note that the perpetual cost reduction is DPS as they take advantage of ever-decreasing silicon geometries, but balance this against the huge processing task which is needed.

*Is this the most effective solution? Is this the most efficient architecture? What are the alternatives?* From first principles it seems obvious that some analog filtering, when performed upon a signal before digitizing, will provide a better starting point. Less noise and better signal to

noise ratio are both an advantage to any subsequent digital processing. Much of the overhead caused by large, long and complex signal paths multiply and accumulate. Signal paths performing basic filtering will be removed freeing up DSP capacity for other tasks or perhaps allowing a smaller DSP to be used; and significantly reducing the number of MIPS and power consumption needed.

#### **What would this Analog Filter Look Like?**

Many optimum filters could be constructed, one for each sub-carrier frequency pair and sequentially switched or multiplexed in and out of the receive channel as required. Obviously, in practice, such a solution would be large, costly and would contain undesirable electrical characteristics after every multiplexing action.

Perhaps a better initial baseband analog solution is a programmable filter. It would need to vary a bandpass filter and gain quickly without circuit interruption (we don’t want transients), and would track the specific frequency expected from specific tags within the reader’s field of view.

#### **Why is this not the Preferred Solution Already?**

Fast dynamically programmable analog filters are not easy to find, nor have they been easy to use. This changed this year when one suitable device became available from Anadigm. Are we now at a time where programmable analog ICs truly complement DSP?

An RFID reader has an inherent knowledge of what type of tag it is expecting to read and at what sub-carrier frequency it will respond because of the communication protocols defined within the various standards. And, of course, readers need to send an instruction to most tag types before they respond. It is therefore relatively easy for a reader’s host processor to control a programmable baseband filter in real time and optimize for the expected sub-carrier receive frequency based upon the tag pre-amble instructions currently being transmitted to the tag.

The benefits of such filter optimization are obvious. Analog filters reject almost all unwanted signal noise, be it from unwanted tags, other

equipment using the same carrier, or backgroundnoise (i.e. fluorescent lights). A cleaner signal from an analog filter means that the subsequent digital processing is much simpler. We can expand this thought all the way to a point where a simple comparator, which follows the filtering and some gain, would be sufficient to square up a waveform and provide a small microprocessor with an input signal which is only needed to perform basic timing upon to extract the data (is it a long pulse or a short one); thus, we have used the same radio and analog baseband signal-process circuit and replaced a complex DSP with a simple uP — good enough for short-range readers.

Alternatively, take the analog signal from the filter and digitize this to perform much more interesting DSP algorithms within the newly available processing bandwidth, i.e. I/Q correlation algorithms, statistical confidence factors and additional filtering.

The concept outlined above can be expanded to include several RF radio front ends (see Figure 2).

Here, a simple switch is used at a non-critical node within the receive channel signal path to choose in some pre-ordained order which of two or more front-end radios are attached sequentially to the baseband signal processor and subsequent digital signal processing.

Given that most RFID tags use the same type of pseudo FSK signaling and that analog filters within the baseband signal processor can be adjusted to optimally match the receive channel sub-carrier frequency at the same time, the input signal path is selected and a low cost multi-radio architecture is realized. Thus, a Universal RFID reader can be constructed with a uP or DSP host controller containing the required protocol stack for multiple tag type and sub-carrier frequencies. This reader has a common analog baseband circuit (controlled by the host) and the minimal signal path duplication as the RF radio front ends.

#### **WD&D**

#### **About the Author**

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